CURRICULUM VITAE

PERSONAL INFORMATION

Name - **BROKALAKIS ANDREAS**

Address - **PLATONOS 4D, CHANIA, CRETE, GREECE**

Telephone Number - **+30 6978113289 (cellphone)**

E-mail - **abrokalakis@ieee.org**

Citizenship - Greek

Place and Date of Birth - Chania, Crete, Greece / November 11th, 1980

STUDIES

2013 – present - School of Electronic and Computer Engineering, Technical University of Crete
PhD Student

2004 - 2007 - Computer Engineering and Informatics Department, School of Engineering – University of Patras
Postgraduate Course : "Integrated Hardware / Software Systems"
M.Sc. Degree : 9.21 / 10 (First Honours – ranked 1st)

1998 - 2004 - Computer Engineering and Informatics Department, School of Engineering – University of Patras
Diploma Degree : 8.50 / 10 (First Honours)
(Note: engineering diplomas in Greece are a result of 5-year academic studies including a research thesis and are certified as equal to Master's degrees)

1995 - 1998 - 3rd Lyceum, Chania, Crete, Greece
Final GPA : 19.2 / 20

FOREIGN LANGUAGES

English - Proficiency in English, University of Cambridge

French - Certificat de Langue Francaise (DELF 1 : Unite A1, A2, A3, A4) , DELF 2 : Unite A5, A6

DISTINCTIONS – SCHOLARSHIPS

- Scholarship from EPEAEK II (National Academic Grant) for my postgraduate studies
- 3rd Prize at the Web Design Competitions – Computer Engineering and Informatics Dept. 2003
- Member of the Parliament of Youth (2nd Summit) after distinction (ranked 1st) in the competition organized by the Hellenic Parliament
- Participated at the Euroscola program of the European Parliament after distinction at the relevant competition
- Distinctions at the competitions of the Hellenic Mathematic Society

PUBLICATIONS

(newest to oldest)

29 C. Diktopoulos, K. Georgopoulos, A. Brokalakis, G. Christou, G. Chrysos, I. Morianos, S. Ioannidis, "Assessing the Effectiveness of Active Fences Against SCAs for Multi-Tenant FPGAs", to appear in International Conference on Field Programmable Logic and Applications (FPL 2022), August 2022.

28 D. Theodoropoulos, A. Brokalakis, N. Alachiotis, D. Pnevmatikatos, "EDRA: A Hardware-assisted Decoupled Access/Execute Framework on the Digital Market", 2021 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS XXI), July 2021

27 N. Alachiotis, A. Brokalakis, V. Amourgianos, S. Ioannidis, P. Malakonakis and T. Bokalidis, "Accelerating Phylogenetics using FPGAs in the Cloud", IEEE Micro, July/August 2021, Vol. 41, Issue 4.

26 P. Malakonakis, A. Brokalakis, N. Alachiotis, E. Sotiriades, A. Dollas, "Exploring Modern FPGA Platforms for Faster Phylogeny Reconstruction with RAxML", 20th IEEE International Conference on Bioinformatics and Bioengineering (BIBE), Virtual Conference, USA, October 2020.

25 N. Tampouratzis, I. Papaefstathiou, A. Nikitakis, A. Brokalakis, St. Andrianakis, A. Dollas, M. Marcon, E. Plebani, "A Novel, Highly Integrated Simulator for Parallel and Distributed Systems", ACM Transactions on Architecture and Code Optimization (ACM TACO), Vol. 17, No. 1, Article 2,

March 2020.

24 P. Toupas, A. Brokalakis, Y. Papaefstathiou, “Accelerating Physics Engine Components with Embedded FPGAs”, 29th Conference on Field-Programmable Logic and Applications (FPL 2019), Barcelona, Spain, September 2019.

23 A. Brokalakis, D.P. Pau, M. Marcon, M. Paracchini, E. Plebani, Y. Papaefstathiou, A. Nikitakis, N. Tampouratzis, St. Andrianakis, R. G. Prajith, I. Sourdis, M. C. Palacios, M. A. Anton and A. Szasz, “COSSIM: An Open-Source Integrated Solution to Address the Simulator Gap for Systems of Systems”, Euromicro Conference on Digital System Design (DSD) 2018, Prague, Czech Republic, August 2018.

22 C. B. Ciobanu, G. Stramondo, A. L. Varbanescu, A. Brokalakis, A. Nikitakis, L. Di Tucci, M. Rabozzi, L. Stornaiuolo, M. Santambrogio, Gr. Chrysos, Ch. Vatsolakis, G. Charitopoulos, D. Pnevmatikatos, “EXTRA: An Open Platform for Reconfigurable Architectures”, International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS 2018), Samos island, Greece, July 2018.

21 A. Brokalakis, A. Nikitakis, I. Papaefstathiou, N. Tampouratzis, St. Andrianakis, A. Dollas, M. Paracchini, M. Marcon, D.P. Pau, E. Plebani, “An Open-Source, Extendable, Highly-Accurate and Security-Aware Simulator for Cloud Applications”, 21st Conference on Innovation in Clouds, Internet and Networks (ICIN 2018), Paris, France, February 2018.

20 A. Brokalakis, I. Chondroulis, I. Papaefstathiou, “Extending the Forward Error Correction Paradigm for Multi-Hop Wireless Sensor Networks”, 9th International Conference on New Technologies, Mobility & Security (NTMS’2018), Paris, France, February 2018.

19 M. Rabozzi, R. Brondolin, G. Natale, E. Del Sozzo, M. Huebner, A. Brokalakis, C. Ciobanu, D. Stroobandt, M. D. Santambrogio, “A CAD Open Platform for High Performance Reconfigurable Systems in the EXTRA Project”, IEEE Computer Society Annual Symposium on VLSI 2017 (ISVLSI2017), Bochum, Germany, July 2017.

18 N. Tampouratzis, A. Nikitakis, A. Brokalakis, St. Andrianakis, I. Papaefstathiou, A. Dollas, “An Open-Source Extendable, Highly-Accurate and Security Aware CPS Simulator”, International Conference on Distributed Computing in Sensor Systems 2017 (DCOSS2017), Ottawa, Canada, June 2017.

17 D. Stroobandt, C. B. Ciobanu, M. D. Santambrogio, G. Figueiredo, A. Brokalakis, D. Pnevmatikatos, M. Huebner, T. Becker, A. J. W. Thom, “An open reconfigurable research platform as stepping stone to exascale high-performance computing”, Design, Automation & Test in Europe 2017 (DATE 2017), Lausanne, Switzerland, March 2017.

16 D.Stroobandt, A. L.Varbanescu, C. B. Ciobanu, M. Al Kadik, A. Brokalakis, G.Charitopoulos, T. Todman, X. Niu, D.Pnevmatikatos, A. Kulkarni, E.Vansteenkiste, W.Luk, M. D. Santambrogio, D.Sciuto, M. Huebner, T. Becker, G.Gaydadjiev, A.Nikitakis, A. J. W. Thom, “EXTRA: Towards the Exploitation of eXascale Technology for Reconfigurable Architectures”, 11th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC 2016), Tallin, June 2016.

15 A. Kulkarni, E. Vansteenkiste, D.Stroobandt, A. Brokalakis, A. Nikitakis, ‘‘A fully parameterized Virtual Coarse Grained Reconfigurable Array for High Performance Computing Applications”, 23rd Reconfigurable Architectures Workshop (RAW 2016), 2016 IEEE International Parallel and Distributed Processing Symposium Workshops, Chicago, May 2016.

14 C. B.Ciobanu , A. L.Varbanescu, D.Pnevmatikatos, G.Charitopoulos, X.Niu , W.Luk, M. D.Santambrogio , D.Sciuto, M. Al Kadi, M. Huebner, T. Becker, G. Gaydadjiev, A. Brokalakis, A.Nikitakis, A.J. W. Thom, E.Vansteenkiste, and D.Stroobandt, “EXTRA: Towards an Efficient Open Platform for Reconfigurable High Performance Computing”, 18th IEEE International Conference on Computational Science and Engineering (CSE-2015), Porto, October 2015

13 D. Pnevmatikatos, K. Papadimitriou, T. Becker, P. Böhm, A. Brokalakis, K. Bruneel, C. Ciobanu, T. Davidson, G. Gaydadjiev, K. Heyse, W. Luk, X. Niu, I. Papaefstathiou, D. Pau, O. Pell, C. Pilato, M.D. Santambrogio, D. Sciuto, D. Stroobandt, T. Todman, E. Vansteenkiste, "FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration", Microprocessors and Microsystems: Embedded Hardware Design (MICPRO) Journal, Available online 6 November 2014, ISSN 0141-9331, http://dx.doi.org/10.1016/j.micpro.2014.09.006.

12 F. Spada, A. Scolari, G.C. Durelli, R. Cattaneo, M.D. Santambrogio, D. Sciuto, D.N. Pnevmatikatos, G.N. Gaydadjiev, O. Pell, A. Brokalakis, W. Luk, D. Stroobandt, D. Pau, "FPGA-Based Design Using the FASTER Toolchain: The Case of STM Spear Development Board", 2014 IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA), Milan, Italy, August 2014

11 D. Pnevmatikatos, T. Becker, A. Brokalakis, G. Gaydadjiev, W. Luk, K. Papadimitriou, I. Papaefstathiou, O. Pell, C. Pilato, D. Pau, M. D. Santambrogio, D. Sciuto, D. Stroobandt, "Effective Reconfigurable Design: the FASTER Approach", Proc. 10th International Symposium on Applied Reconfigurable Computing (ARC), Vilamoura, Algarve, Portugal, April, 2014

10 L. Lavagno, M. Lazarescu,I. Papaefstathiou, A. Brokalakis, J. Walters, B. Kienhuis, Fl. Schaefer,

"HEAP: a Highly Efficient Adaptive multi-Processor framework", Microprocessors and Microsystems: Embedded Hardware Design (MICPRO) Journal, vol. 37, issue 8, pages 1050 - 1062, 17 November 2013, ISSN 0141-9331

9 D. Pnevmatikatos, T.Becker, A. Brokalakis, K. Bruneel, G. Gaydadjiev, W. Luk, K. Papadimitriou, I. Papaefstathiou, O. Pell, Chr. Pilato, M. Robart, M. Santambrogio, D. Sciuto, D, Stroobandt and T. Todman, "FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration", 15th Euromicro Conference on Digital System Design (DSD 2012), Izmir, Turkey, September 2012.

8 L. Lavagno, M. Lazarescu, J. Walters,B. Kienhuis, I. Papaefstathiou, A. Brokalakis, Fl. Schaefer, "HEAP: a Highly Efficient Adaptive multi-Processor framework", 15th Euromicro Conference on Digital System Design (DSD 2012), Izmir, Turkey, September 2012.

7 A. Brokalakis, I. Papaefstathiou, "Using Hardware-Based Forward Error Correction to Reduce the Overall Energy Consumption of WSNs", 2012 IEEE Wireless Communications and Networking Conference (WCNC 2012), Paris, France, April 2012.

6 K. Papadopoulos, A. Brokalakis, I. Papaefstathiou, "Increasing Resistance to Differential Power Analysis Attacks in Reconfigurable Systems", 16th IEEE Mediterranean Electrotechnical Conference (MELECON 2012), Medina Yasmine Hammamet, Tunisia, March 2012.

5 G. Chatziparaskevas, A. Brokalakis, I. Papaefstathiou, "An FPGA-based Parallel Processor for Black-Scholes Option Pricing Using Finite Differences Schemes", Design, Automation and Test in Europe 2012 (DATE 2012), Dresden, March 2012.

4 A. Brokalakis, V. Paliouras, "Using the Arithmetic Representation Properties of Data to Reduce the Area and Power Consumption of FFT Circuits for Wireless OFDM Systems", IEEE Workshop on Signal Processing Systems (SiPS2011), Beirut, October 2011.

3 A. Brokalakis, G.-Gr. Mplemenos, K. Papadopoulos, I. Papaefstathiou, "RESENSE: An Innovative, Reconfigurable, Powerful and Energy Efficient WSN Node", IEEE International Conference on Communications 2011 (ICC2011), Kyoto, Japan, June 2011.

2 G.-Gr. Mplemenos, Konstantinos P, A. Brokalakis, Gr. Chrysos, E. Sotiriades, I. Papaefstathiou, "RESENSE: Reconfigurable WSN nodes", Wireless Sensing Showcase, London, July 2009.

1 A. Brokalakis, A. Kakarountas, C. Goutis, "A High-Throughput Area Efficient FPGA Implementation of AES-128 Encryption", IEEE Workshop on Signal Processing Systems (SiPS2005), Athens, November 2005.

REVIEWER AT CONFERENCES/JOURNALS

- Reviewer for USENIX 2021 and USENIX 2022
- Reviewer for the IEEE Transactions on Wireless Communications, IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, ACM Transactions on Reconfigurable Technology and Systems
- Reviewer for the Design, Automation and Test in Europe Conference 2017 (DATE 2017)
- Member of the Technical Program Committee of the IEEE AFRICON 2015 conference
- Reviewer for the IEEE International Symposium on Circuits and Systems 2013 (ISCAS 2013).
- Reviewer for the International Conference on Field Programmable Logic and Applications (FPL) 2012 - 2018
- Reviewer at the Communication Theory Symposium of the IEEEGlobal Communications Conference 2010 (GLOBECOM 2010).

MASTER THESIS

Title - "*Low-power VLSI Modem Architectures for Wireless OFDM Networks: the Role of Alternative Computer Arithmetic*"

Supervisor - Prof. Paliouras Vassilis

Work Outline - Study of the arithmetic behavior of data for a 64-point FFT for OFDM modems and devise of proper arithmetic representations based on BER performance in an OFDM receiver. Design of a radix-8 row-column 64-point FFT architecture using 2's complement arithmetic and hybrid 2's complement and Logarithmic Numbering System (LNS) arithmetic. Performance, area and power comparisons between implementations. Synthesis using Synopsys Design Compiler for .18μm CMOS standard-cell library (UMC). Power estimations using ModelSim and Synopsys Power Compiler.

DIPLOMA THESIS

Title	-	"*Design of A Dynamic Reconfigurable RISC Processor and Implementation on an FPGA*"
Supervisor	-	Prof. Nikolos Dimitris
Work Outline	-	Design of a 32-bitRISCProcessor with a Dynamic Reconfigurable FPU. Implementation on a Xilinx Virtex FPGA. Development of an assembler to translate assembly code to machine code (in C). Development of Integer routines to simulate FP Instructions (in Assembly to be used internally in the processor). Development of a cycle accurate Processor Simulator (in C).

WORK EXPERIENCE

March 2015 – present	-	Linux System Administrator for the servers of the Microprocessor and Hardware Laboratory (MHL) of Electronics and Computer Engineering School, Technical University of Crete
December 2019 – present	-	Research Associate, Institute of Computer Science, Foundation of Research and Technology (FORTH). *Current Position*: Researcher for the EU research project H2020 COLLABS (A COmprehensive cyber-intelligence framework for resilient coLLABorative manufacturing Systems)
October 2008 – present	-	Research Associate / Engineer, Telecommunication Systems Institute (http://www.tsi.gr) / Microprocessor and Hardware Laboratory (MHL), Electronics and Computer Engineering School, Technical University of Crete. *Most recent positions*: Researcher: H2020 IntelIIoT, Researcher / Hardware Developer for the H2020 EDRA EU FET Innovation Launchpad Project.
February 2010 – September 2019	-	Senior Computer Engineer, Synelixis Solutions Ltd (http://www.synelixis.com) European Union research projects: September 2015 – October 2019: H2020 EXTRA (Exploiting eXascale Technology with Reconfigurable Architectures), https://www.extrahpc.eu/ February 2015 – February 2018: H2020 COSSIM (A Novel, Comprehensible, Ultra-Fast, Security-Aware CPS Simulator) - http://www.cossim.org/ September 2011 – January 2015: FP7 FASTER (Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration) – http://www.fp7-faster.eu February 2010 – March 2013: FP7 HEAP (Highly Efficient Adaptive multi-Processor framework) – http://www.synelixis.com/portfolios/heap
June 2006	-	Design and implementation of the personal website of the photographer Rainer Pawellek. (http://perso.orange.fr/rainer.pawellek/)
Academic Year 2014-2015 / 2016-2017	-	Lab Assistant for the course "Embedded Systems" (7th semester, School of Electronic and Computer Engineering, Technical University of Crete)
Academic Year 2013-14 / 2016-17/ 2017-18	-	Lab Assistant for the course "Computer Architecture" (8th semester, School of Electronic and Computer Engineering, Technical University of Crete)
Academic Year 2000-2001 / 2004-2005	-	Supervisor of the Computer Architecture Lab (3rd semester, Computer Engineering and Informatics Dept., University of Patras)
Academic Year 2004-2005	-	Supervisor of the Electronics Lab (3rd semester, Computer Engineering and Informatics Dept., University of Patras)

TECHNICAL SKILLS

Programming Languages	C/C++ (pthreads, OpenMP, MPI, OpenCL), Java, Assembly, SQL, nes-C / programming for HPC and embedded systems, linux development (applications and system level)
MarkUp Languages	HTML/CSS, XML, XSLT
Scripting Languages	Python, Javascript, PHP, bash/tcsh shell scripting
Hardware Description Languages	Verilog/System Verilog HDL, Vivado HLS (High Level Synthesis)
Technical Languages	Matlab, Maple
Operating Systems	MS-Windows, Solaris, Linux, RT-Linux (real time)
System Administration	Linux Server Administrator (CentOS/RedHat, Ubuntu)
Most Important Software Packages	MS Office/Visio/Visual Studio, gcc/gdb/gprof/Valgrind, MathWorks Matlab, Mentor Graphics ModelSim, Xilinx ISE/Vivado/SDAccel/SDSoC, Synopsys Design Compiler, Intel Parallel Studio, Petalinux, Wordpress

PROJECTS

These are the most important projects that I have completed and provide proof on my technical skills. Projects are separated in two groups, one for the ones completed during my under/post-graduate studies and one for the ones in my work.

Work Projects

Wireless Sensor Networks / Hardware Design	- Design of a Turbo Code Encoder for wireless sensor networks. Implementation on CrossBow (MICAz and IRIS) motes in software (nesC – TinyOS) and in hardware attached to those motes (on a Xilinx CPLD / Verilog HDL). Real-world energy measurements of the two implementations. This work was carried out for the EU-funded research project FP7 – Ad-Hoc PAN and Wireless Sensor Secure NETwork (AWISSENET). Associated publications 2, 3 and 7. - Design of a matching Turbo Code Decoder for central nodes in extended star topology for WSNs. This work has been the diploma thesis of a Technical University of Crete student under my supervision. Our work resulted in publication 20.
Bluetooth Proximity Advertising	- Programming of a Bluetooth Access Server for a Proximity Advertising application for Bluetooth-enabled cellphones. (Embedded Linux, bash scripting, C). Work under contract for Telecommunication Systems Institute.
FPGA Hardware Design	- Development of an FPGA accelerator for solving tridiagonal systems used in Option Pricing calculations (C/C++, Verilog, XilinxVirtex-5/6FPGAs). Associated publication 5. - Development of a reconfigurable (micro/dynamic partial) Network Intrusion Detection System (NIDS) for Gigabit Ethernet networks based on the Snort system (C, Verilog/VHDL, Xilinx Virtex 5 FPGAs). This work was carried out for the EU-funded research project FP7 – FASTER. Associated publications for the project: 9, 11, 12, 13. - Development of a retinal image segmentation application for Zynq and Zynq Ultrascale devices (software / hardware codesign). Implementation using Vivado HLS. This work is carried out in the context of EU-funded research project H2020 EXTRA. Associated publications for the project: 14, 15, 16, 17, 19 and 22. - Design and development of an accelerator for the Bullet Physics Engine open source library using Xilinx MPSoc Zynq US+ devices. This work has been the diploma thesis of a Technical University of Crete student under my supervision. Our work resulted in publication 24. - Development of an FPGA accelerator for the phylogenetics analysis application RAxML. The accelerator is implemented on the F1 instances of the AWS cloud. This work has been carried out for the EU-funded project H2020 EDRA. Associated publications 26, 27.
Microprocessor System Design / Computer Architecture / Hardware Design	- Development of a multi-core processor (4/8/16/24 cores) based on the Xilinx MicroBlaze microprocessor and implementation of custom cache coherency protocols based on snooping and VIPS schemes. Implementation on Virtex-6 FPGAs of the overall multiprocessor (including CPU cores, custom caches, interrupt controllers, interconnection network, peripherals, memory subsystem, basic I/O and debugging cores). Implementation of support software tools (such as extensions to XilKernel to include multiprocessor support, basic low-level software for system initialization and testing) and software applications for testing and performance measurements. Hardware development in Verilog and custom scripts for system development in Xilinx EDK, software development in C (Xilinx SDK, XilKernel) This work was carried out for the EU-funded research project FP7 – HEAP. Associated publications: 8 and 10. - Development of the COSSIM Simulation Framework. The COSSIM simulation framework extends the architectural full system simulator GEM5 enabling it to simulate parallel and networked systems in general. GEM5 is interconnected through HLA with OMNET++ network simulator and a distributed simulation system is formed. Additional work within COSSIM is the extension of McPAT (power/energy estimator) that is integrated in the framework. Several modifications have been made in McPAT that provide higher accuracy results and enable the estimator to be used for all processor models supported in COSSIM. The overall COSSIM framework has been developed in EU-funded research project H2020-COSSIM and is available as an open source package in GitHub here: https://github.com/H2020-COSSIM. Associated publications: 18, 21, 23 and 25.

Projects completed during my studies

Hardware Design	- Design of a voice CODEC based on CVSD algorithm with programmable settings. (in Verilog HDL, targeting Altera FPGAs) - Gate-Level Design of Arithmetic Circuits for various Computer Arithmetic Systems (Sign-Magnitude, 2's Complement, LNS, RNS) - Architectural design of various DSP systems. - Implementation of a Scheduler for a 4x4 Router based on the FIRM Algorithm (in Verilog HDL, targeting Xilinx Spartan FPGAs) - Implementation of an Embedded FPGA-Accelerated System in a Zynq SoC (ARM A9 + FPGA) (Vivado HLS, Vivado), Generation of a proper linux system and device drivers (Petalinux)

Parallel Systems	-	Computation Acceleration through parallelization using OpenMP, pthreads, MPI and vectorization through SSE/SSE4/AVX/AVX2 intrinsics
Computer Architecture	-	Optimization of the Implementations of the Cache Memory Model of the SimpleScalar Simulator to increase simulator's performance in cache-decay schemes (in C)
Telecommunications	-	Implementation of a Forward Linear Predictor & Echo Canceller (in MATLAB)
	-	Simulations & Experimental Evaluation of a BaseBand Telecommunication System (PAM) (in MATLAB)
Digital Signal Processing	-	Implementation of the Adaptive Filters LMS and RLS (in MATLAB) System Modeling according to AR and MA, Evaluation of the Power Spectrum of a Stochastic Process (in MATLAB)
	-	Implementation of Audio Effects (Echo, Reverb, Flanger, Chorus) (in MATLAB)
	-	Voice signal Compression using Sub-Band Coding (in MATLAB)
Digital Image Processing	-	Implementation of 2D FFT / 2D DCT Transformations, Image Restoration (Average – Median Filters), Homomorphic Filtering (using Butterworth first order filters), Inverse / Wiener Filters, Edge Detection (using Sobel operator), Total Histogram Equalization for Color Images (in RGB and HSV)(in MATLAB)
Network Programming	-	Implementation of a File-Sharing Application using a central server (Peer-To-Peer Application – Development of the Central Server as well as the Client/Server applications) (in C, for Unix/Linux OSes)
	-	Implementation of a Multithreaded Application Server for fleet management (in C++, Linux, POSIX Threads)
Software Architecture	-	Modeling of a QoS Manager for a real-time embedded system using UML.
Operating Systems	-	Linux Shell Scripting, Virtual File System, implementation of new Signals and new System Calls
Neural Networks	-	Implementation of a back-Propagation algorithm in a Multilayer Feed-Forward Neural Network (in MATLAB)
Compilers	-	Implementation of an HTML parser (in C, using Flex and Bison)
Web Development	-	Implementation of a Content Management System for a Web Directory for Companies (Server Side : Web Server : Apache, Data Base : MySQL, Server Side Scripting : PHP Client Side : HTML/CSS, XML/XSLT, Javascript)

SEMINARS

Title	-	InTraLED – Training in Low Power Design, 4rth Course "*Low Power Issues in VLSI Testing and Design for Testability"*
Organizer		*University of Patras*
Dates		December 2004 - February 2005
Title	-	InTraLED – Training in Low Power Design, 3rd Course "*System-Level Design for Low Power"*
Organizer		*University of Patras*
Dates		15 - 17November 2004
Title		InTraLED – Training in Low Power Design, 2nd Course "*Power Modelling and Estimation of Digital Circuits – Techniques and Tools"*
Organizer		*University of Patras*
Dates		19 - 21October 2004
Title	-	InTraLED – Training in Low Power Design, 1st Course "*Design of low-power digital circuits – Techniques and Tools"*
Organizer		*University of Patras*
Dates		20 - 22 September 2004

OTHER

Professional Licenses	-	Member of the Hellenic Technical Chamber since March 2007
	-	Member of the Institute of Electrical and Electronics Engineers (IEEE) - Circuits and Systems (CAS) Society, Computer (CS) Society and Communications (ComSoc) Society
Army Service	-	Completed (August 2007 – August 2008, Technical Corpse, Telecommunications Technician)
Music Studies	-	Music Theory (Harmony, Solfeze), Classic / Electric Guitar (Venizelio Conservatory of Chania)
Photography	-	Photo/Travel blog: https://www.croissantstories.com Participated in the following Group Photography Exhibitions:

- *Photography Exhibition for the 50 Years Since the Establishment of the Samaria National Park,* Neorio of Moro, Chania Sailing Club, August- September 2012.
- *Photography Festival "Fotoskiaseis 2012"*, Neorio of Moro, Chania Sailing Club, May 2012
- *Group Photography Exhibition "Public Spaces"* – Neorio of Moro, Chania Sailing Club, June 2011
- *Group Photography Exhibition,* Immigrants House of Chania, March 2010
- *Fotoskiasis 2009*, Koundourou Villa, May 2009
- *Photography Weekend*, School of Architecture, Technical University of Crete, June 2008
- *Photography Festival*, Old Arsakeio of Patras, May 2007
- *Artware Festival 2006*, Computer Engineering and Informatics Dept. – University of Patras,

Workshops :

- participating under scholarship at the Documentary Project Photography WorkShop, Maine Media Workshops (instructor: Stella Johnson), Chania, May 2009.
- Teaching Assistant, Documentary Project Photography WorkShop, Maine Media Workshops (instructor: Stella Johnson), Chania, May/June 2008.

Driving Licenses - Motorcycle, car, motor boat